Hall Ticket Number:

Code No. : 17453 (A) N/O

VASAVI COLLEGE OF ENGINEERING *(AUTONOMOUS)*, HYDERABAD

Accredited by NAAC with A++ Grade

B.E. (E.C.E.) VII-Semester Main & Backlog Examinations, Dec.-23/Jan.-24

Advanced Embedded Systems (PE-II)

Time: **3 hours** Max. Marks: **60**

*Note: Answer all questions from **Part-A** and any **FIVE** from **Part-B***

Part-A (10 × 2 = 20 Marks)

Q. No.	Stem of the question	M	L	CO	PO	PSO
1.	List any two differences between Embedded System and General-Purpose Computing system.	2	1	1	1	1
2.	Calculate the percentage of revenue loss due to a delay of 3 months in completing an embedded project, whose maximum sales is predicted to occur on 18th month?	2	2	1	2	1
3.	Differentiate between hard-view license and soft-view license offerings by ARM to different design firms?	2	3	2	3	2
4.	Which aspects are significant in ARM Cortex-M compared with ARM Cortex-A CPU cores?	2	2	2	1	1
5.	What is the three-wire protocol? Mention any two applications of it in the embedded systems?	2	1	3	1	1
6.	Draw the circuit diagram of interfacing CMOS UART to RS232 port of a 4G modem?	2	3	3	3	1
7.	Draw the flowchart of hardware/software codesign for designing an embedded system.	2	2	4	2	1
8.	Mention the advantage and disadvantage of Functional Queue Scheduling Algorithm compared with Round Robin and RR with interrupt driven architectures.	2	3	4	2	1
9.	Differentiate between Compiler and Cross Compiler? Give an example of Cross Compiler IDE used in embedded system?	2	2	5	2	1
10.	Pack the32-bit instruction 0x1234ABCD into 16-bit Flash in Little-endian and Big-endian formats?	2	3	5	3	1
	Part-B (5 × 8 = 40 Marks)					
11. a)	Define and distinguish between hard real-time system and soft real-time system. Support your answer with a suitable timing diagram?	4	1	1	2	1
b)	Explain the important aspects that needs to be considered while selecting a CPU for designing an embedded system.	4	2	1	3	1
12. a)	Explain different registers of ARM in different modes with a suitable diagram and draw the CPSR register format?	4	3	2	1	1

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b)	Sketch the ARM CPU engine architecture and discuss the significance of Baral Shift Register?	4	2	2	1	1
13. a)	What is the unique differentiating principle of CAN protocol compared with other serial protocols? Explain CAN 2.0B frame format, indicating each field.	4	2	3	4	2
b)	Explain the working principle of SPI protocol? Draw its three-stage daisy-chain configuration?	4	3	3	2	3
14. a)	Define hardware/software Codesign. Considering the case study of designing an ECU (Electronic Control Unit) for Adaptive Cruise Control (ACC), explore the different options of hardware and software modules.	4	3	4	4	2
b)	Is polled loop system same as Round Robin scheduling algorithm? Justify your answer with the help of Pseudo code implementation?	4	2	4	2	3
15. a)	Discuss different stages of converting an application implemented either in embedded-C or in embedded-C++ into the target-specific hardware executable with suitable diagram?	4	1	5	4	2
b)	Specify the requirement(s), where user can configure interrupt as edge triggered or level-triggered? List any four important aspects of writing an efficient Interrupt Service Routine (ISR)?	4	3	5	5	2
16. a)	Define an Embedded System. Based on size and cost, illustrate different classifications of embedded systems and mention one example embedded system under each category.	4	1	1	1	1
b)	What is AMBA bus? With the help of a block diagram, indicate the significance of APB and ASB.	4	2	2	2	1
17.	Answer any ***two*** of the following:					
a)	Explain the working principle of I^2C? What are the different states that a Microcontroller will undergo during I^2C communication?	4	3	3	2	1
b)	Discuss the implementation aspects of Interrupt-driven Round Robin scheduling architecture by considering three asynchronous external interrupts for an embedded system. Compare its Merits and demerits with polled loop system.	4	3	4	3	2
c)	Illustrate different software methods or tools for debugging an embedded application?	4	2	5	2	1

M : Marks; L: Bloom's Taxonomy Level; CO; Course Outcome; PO: Programme Outcome

i)	Blooms Taxonomy Level – 1	20%
ii)	Blooms Taxonomy Level – 2	40%
iii)	Blooms Taxonomy Level – 3 & 4	40%

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